CLAIMS

1. A semiconductor device comprising a first semiconductor region and a second semiconductor region,

(a) wherein a field effect transistor is comprised of the first semiconductor region comprising at least one semiconductor layer(s) protruding upward from a substrate, a gate electrode(s) formed via an insulating film such that the gate electrode(s) strides over the semiconductor layer(s) and source/drain regions provided in the semiconductor layer(s) on both sides of the gate electrode(s),whereby a channel region is formed in at least both side surfaces of the semiconductor layer(s),

(b) wherein the second semiconductor region comprises semiconductor layers protruding upward from the substrate and placed, at least opposing the first semiconductor region at both ends in the direction perpendicular to a channel current direction and the side surfaces of the semiconductor layers facing the first semiconductor region are parallel to the channel current direction.

2. The semiconductor device as claimed in Claim 1, wherein the first semiconductor region comprises a plurality of the semiconductor layers aligned such that the channel current direction is mutually parallel.

3. The semiconductor device as claimed in Claim 2, wherein separate source/drain regions and separate gate electrodes are formed to each of the plurality of the semiconductor layers in the first semiconductor region.

4. The semiconductor device as claimed in Claim 2, wherein the gate electrode(s) is formed such that the gate electrode(s) strides over at least two of the plurality of the semiconductor layers.

5. The semiconductor device as claimed in Claim 2, wherein individual source/drain regions in the plurality of the semiconductor layers are electrically commonly connected and the gate electrode(s) is formed such that the gate electrode(s) strides over the commonly connected semiconductor layers.

6. The semiconductor device as claimed in Claim 2, wherein the first semiconductor region further comprises a connecting semiconductor layer which protrudes upward from the substrate and electrically commonly connects source/drain regions of at least two of the plurality of the semiconductor layers by extending in the direction perpendicular to the channel current direction; and

the gate electrode(s) is formed such that the gate electrode(s) strides over the semiconductor layers connected by the connecting semiconductor layer.

7. The semiconductor device as claimed in any of Claims 2 to 5, wherein in the direction perpendicular to the channel current direction, an additional semiconductor layer in the second semiconductor region is formed between the plurality of the semiconductor layers in the first semiconductor region.

8. The semiconductor device as claimed in any of Claims 2 to 6, wherein the plurality of the semiconductor layers are aligned at even intervals in the direction perpendicular to the channel current direction.

9. The semiconductor device as claimed in any of Claims 1 to 8, wherein the semiconductor layers in the second semiconductor region formed in both sides of the first semiconductor region are disposed at even intervals from the first semiconductor region.

10. The semiconductor device as claimed in any of Claims 1 to 9, wherein the semiconductor layer(s) in the first semiconductor region and the semiconductor layers in the second semiconductor region are aligned at even intervals in the direction perpendicular to the channel current direction.

11. The semiconductor device as claimed in any of Claims 1 to 10, wherein the gate electrode(s) is formed, extending from over the semiconductor layer(s) in the first semiconductor region to over the semiconductor layers in the second semiconductor region.

12. The semiconductor device as claimed in Claim 11, wherein a contact with the gate electrode(s) is formed over the semiconductor layers in the second semiconductor region.

13. The semiconductor device as claimed in any of Claims 1 to 12, wherein at least a part covered by the gate electrode(s) in the semiconductor layer(s) in the first semiconductor region has a substantially cuboid shape.

14. The semiconductor device as claimed in any of Claims 1 to 12, wherein the semiconductor layer(s) in the first semiconductor region has a substantially cuboid shape.

15. The semiconductor device as claimed in any of Claims 1 to 14, wherein in the channel current direction, a length of the semiconductor layers in the second semiconductor region in both sides of the first semiconductor region is longer than a length of the gate electrode(s).

16. The semiconductor device as claimed in any of Claims 1 to 14, wherein in the channel current direction, a length of the semiconductor layers in the second semiconductor region in both sides of the first semiconductor region is equal to or larger than a length of the semiconductor layer(s) in the first semiconductor region.

17. The semiconductor device as claimed in any of Claims 1 to 16, wherein in the direction perpendicular to the channel current direction, a width of the semiconductor layers in the second semiconductor region in both sides of the first semiconductor region is equal to or larger than a width of the semiconductor layer(s) in the first semiconductor region.

18. The semiconductor device as claimed in any of Claims 1 to 17, wherein the second semiconductor region further comprises a pair of semiconductor layers which connects from one semiconductor layer to the other semiconductor layer of the semiconductor layers in both sides of the first semiconductor region such that the second semiconductor region surrounds the first semiconductor region.

19. A process for manufacturing a semiconductor device, comprising the steps of:

forming fin-type semiconductor layers for forming a first semiconductor region comprising at least one semiconductor layer(s) protruding upward from a substrate and a second semiconductor region comprising semiconductor layers protruding upward from the substrate at least in both sides sandwiching the first semiconductor region; and

forming a transistor by forming a gate electrode(s) striding over the semiconductor layer(s) in the first semiconductor region, an insulating film between the gate electrode(s) and at least both side surfaces of the semiconductor layer(s) and source/drain regions in both sides sandwiching the gate electrode(s) in the semiconductor layer(s).

20. The process for manufacturing a semiconductor device as claimed in Claim 19, wherein in the step of forming the fin-type semiconductor layers, the first semiconductor region and the second semiconductor region are formed such that the side surface of the second semiconductor region in the side of the first semiconductor region is parallel to a channel current direction.

21. The process for manufacturing a semiconductor device as claimed in Claim 19 or 20, wherein in the step of forming the fin-type semiconductor layers, the first semiconductor region and the second semiconductor region are

simultaneously formed by processing a semiconductor substrate on the substrate into a predetermined shape.

22. The process for manufacturing a semiconductor device as claimed in Claim 21, wherein in the step of forming the fin-type semiconductor layers, the processing into the predetermined shape is conducted by etching the semiconductor substrate using a mask having a shape corresponding to the first semiconductor region and the second semiconductor region.

23. The process for manufacturing a semiconductor device as claimed in any of Claims 19 to 22, wherein in the step of forming the transistor, the gate electrode(s) is formed such that the gate electrode(s) extends from over the semiconductor layer(s) in the first semiconductor region to over the semiconductor layers in the second semiconductor region.

24. The process for manufacturing a semiconductor device as claimed in Claim 23, wherein in the step of forming the transistor, a contact with the gate electrode(s) is further formed over the semiconductor layers in the second semiconductor region to which the gate electrode(s) extends.

25. The process for manufacturing a semiconductor device as claimed in any of Claims 19 to 24, wherein in the step of forming the fin-type semiconductor layers, a plurality of the semiconductor layers are formed as the first semiconductor region such that direction of channel current flowing in the individual semiconductor layers is mutually parallel.

26. The process for manufacturing a semiconductor device as claimed in Claim 25, wherein in the step of forming the transistor, a plurality of the gate electrodes are formed such that each gate electrode strides over one semiconductor layer in the first semiconductor region.

27. The process for manufacturing a semiconductor device as claimed in Claim 25, wherein in the step of forming the transistor, the gate electrode(s) is

formed such that the gate electrode(s) strides over at least two or more of the plurality of the semiconductor layers in the first semiconductor region.

28. The process for manufacturing a semiconductor device as claimed in Claim 25, wherein in the step of forming the fin-type semiconductor layers, a connecting semiconductor layer is further formed as the first semiconductor region, which protrudes upward from the substrate, extends in a direction perpendicular to the channel current direction and electrically commonly connects at least two of the plurality of the semiconductor layers; and

wherein in the step of forming the transistor, the gate electrode(s) is formed such that the gate electrode(s) strides over the semiconductor layers connected by the connecting semiconductor layer.

29. The process for manufacturing a semiconductor device as claimed in any of Claims 25 to 27, wherein in the step of forming the fin-type semiconductor layers, an additional semiconductor layer in the second semiconductor region is formed between the semiconductor layers in the first semiconductor region.

30. The process for manufacturing a semiconductor device as claimed in any of Claims 25 to 28, wherein in the step of forming the fin-type semiconductor layers, the plurality of the semiconductor layers in the first semiconductor region are formed at even intervals in the direction perpendicular to the channel current direction.

31. The process for manufacturing a semiconductor device as claimed in any of Claims 25 to 30, wherein in the step of forming the fin-type semiconductor layers, the semiconductor layers in the second semiconductor region are disposed in both sides of the first semiconductor region at even intervals from the first semiconductor region.

32. The process for manufacturing a semiconductor device as claimed in any of Claims 25 to 31, wherein in the step of forming the fin-type semiconductor layers, the plurality of the semiconductor layers in the first semiconductor region and the semiconductor layers in the second semiconductor region are formed at even intervals in the direction perpendicular to the channel current direction.

33. The process for manufacturing a semiconductor device as claimed in any of Claims 19 to 32, wherein in the step of forming the fin-type semiconductor layers, at least a part covered by the electrode gate(s) in the semiconductor layer(s) in the first semiconductor region are formed such that the part has a substantially cuboid shape.

34. The process for manufacturing a semiconductor device as claimed in any of Claims 19 to 32, wherein in the step of forming the fin-type semiconductor layers, the semiconductor layer(s) in the first semiconductor region are formed such that the semiconductor layer(s) has a substantially cuboid shape.

35. The process for manufacturing a semiconductor device as claimed in any of Claims 19 to 34, wherein in the step of forming the transistor, the semiconductor layers in the second semiconductor region are formed in both sides of the first semiconductor region such that a length of the semiconductor layers in the channel current direction is longer than a length of the gate electrode(s).

36. The process for manufacturing a semiconductor device as claimed in any of Claims 19 to 34, wherein in the step of forming the transistor, the semiconductor layers in the second semiconductor region are formed in both sides of the first semiconductor region such that a length of the semiconductor

layers in the channel current direction is longer than a length of the semiconductor layer(s) in the first semiconductor region.

37. The process for manufacturing a semiconductor device as claimed in any of Claims 19 to 36, wherein in the step of forming the transistor, the semiconductor layers in the second semiconductor region are formed in both sides of the first semiconductor region such that a width of the semiconductor layers in the direction perpendicular to the channel current direction is equal to or larger than a width of the semiconductor layer(s) in the first semiconductor region.

38. The process for manufacturing a semiconductor device as claimed in any of Claims 19 to 37, wherein in the step of forming the fin-type semiconductor layers, a pair of semiconductor layers are further formed as the second semiconductor region, which connects from one semiconductor layer to the other semiconductor layer of the semiconductor layers in both sides of the first semiconductor region such that the second semiconductor region surrounds the first semiconductor region.